**Amendments to the Claims**

Please cancel claims 16 and 17 without prejudice or disclaimer of the subject matter recited therein. Please amend claims 10, 11, 15, and 35 as shown below.

1. (Previously Presented) A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells in the substrate of the first conductivity type, said charge wells being formed in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap between the at least two gate electrodes; and

a semiconductor region of the first conductivity type, formed in the interelectrode gap, but having a different dopant concentration than the substrate for stabilizing the inter-electrode gap.

2. (Canceled)

3. (Previously Presented) A charge coupled device according to claim 1, wherein the apparatus for stabilizing the inter-electrode gap further includes:

a further dielectric layer formed over the at least two gate electrodes; and

a further gate electrode formed overlying the further dielectric layer and selectively positioned over the inter-electrode gap.

4. - 7. (Canceled)

8. (Previously Presented) A charge coupled device according to claim 1, wherein a first one of the charge well areas and its corresponding gate electrode form a photogate optical sensor and the charge coupled device further comprises:

a charge barrier well of a first conductivity type adjacent to the photogate optical sensor, the charge barrier well being configured to divert photocarriers into at least the photogate optical sensor; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

9. (Previously Presented) A charge coupled device according to claim 8, further including:

a further charge barrier well of the first conductivity type, distal to the photogate optical sensor and the anti-blooming drain; and

a second diffusion region of the second conductivity type in the further charge barrier well, the second diffusion region forming a charge sink, wherein one of the at least two gate

electrodes that is not a photogate optical sensor overlies a portion of the further charge barrier well adjacent to the charge sink.

10. (Currently Amended) A charge coupled device according to claim 9, further comprising a plurality of further diffusion regions of the second conductivity type in the further charge barrier well adjacent to the charge sink and forming a plurality of transistors, wherein the plurality of transistors ~~include~~ includes a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

11. (Currently Amended) An optical sensor circuit for receiving photocarriers from a source and being formed on a single monolithic substrate comprising:

a charge coupled device (CCD) array, the array being formed of a plurality of single polysilicon CMOS pixels, each pixel including,

a semiconductor layer of a first conductivity type formed on the substrate;

a first dielectric layer overlaying the semiconductor layer, the first dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the first dielectric layer and configured to define at least two charge wells, respectively, in the semiconductor layer, in response to a bias potential applied to the at least two gate electrodes, wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap in the semiconductor layer, a combination of one of the at least two charge wells and its respective overlaying gate electrode forming a

photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlaying gate electrode forming a transfer gate; and

a semiconductor region of the first conductivity type, formed in the inter-electrode gap for stabilizing the inter-electrode gap, but having a different dopant concentration than the semiconductor layer~~; and~~.

12. (Canceled)

13. (Previously Presented) An optical sensor according to claim 11, further comprising:

a charge barrier well of the first conductivity type adjacent to the photogate optical sensor, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

14. (Previously Presented) An optical sensor according to claim 13, further including:

a further charge barrier well of the first conductivity type, distal to the photogate optical sensor and the anti-blooming drain; and

a second diffusion region of the second conductivity type in the further charge barrier well, the second diffusion region forming a charge sink, wherein one of the at least two gate electrodes that is not a photogate optical sensor overlies a portion of the further charge barrier well adjacent to the charge sink.

15. (Currently Amended) A charge coupled device according to claim 13, further comprising a plurality of further diffusion regions of the second conductivity type in the further charge barrier well adjacent to the charge sink and forming a plurality of transistors, wherein the plurality of transistors ~~include~~ includes a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

16. (Cancelled)

17. (Cancelled)

18. (Previously Presented) A charge coupled device made according to a standard single polysilicon CMOS process, the charge coupled device comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type;

an oxide layer formed over at least the well region, the oxide layer being a CMOS gate oxide layer;

first and second polysilicon gate electrodes formed on the oxide layer over the well region, the first and second gate electrodes being separated by an inter-electrode gap in the well region, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register; and

a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region for stabilizing the inter-electrode gap, but having a different dopant concentration than the well region.

19. (Canceled)

20. (Previously Presented) A back illuminated imager comprising:

a substrate of a first conductivity type having a front side and a back side;

a CCD pixel structure formed in the front side of the substrate;

a well region of a second conductivity type, opposite to the first conductivity type, formed in the front side of the substrate and separate from the CCD pixel structure, the well region and the substrate forming a semiconductor junction; and

at least one diffusion region in the well region of the second conductivity type forming a component of a back illuminated imager, said CCD pixel structure overlying said at least one diffusion region;

whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction.

21. (Previously Presented) The charge coupled device according to claim 18, further comprising optics that are configured to focus radiation onto the back side of the substrate.

22. - 30. (Canceled)

31. (Previously Presented) The charge coupled device of claim 11, wherein the semiconductor layer is a transmission channel and the transmission channel is a CMOS N-well.

32. (Previously Presented) The charge coupled device of claim 1, wherein the at least two gate electrodes include at least two CMOS polysilicon gate electrodes.

33. (Previously Presented) A charge coupled device according to claim 18, further comprising:

a charge barrier well of a first conductivity type adjacent the first polysilicon gate electrode and distal to the second gate electrode; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

34. (Previously Presented) A charge coupled device according to claim 33, further including:

a further charge barrier well of the first conductivity type adjacent to the second polysilicon gate electrode and distal to the first polysilicon gate electrode and the anti-blooming drain; and

a second diffusion region of the second conductivity type in the further charge barrier well, the second diffusion region forming a charge sink, wherein the second gate electrode overlies a portion of the further charge barrier well adjacent to the charge sink.

35. (Currently Amended) A charge coupled device according to claim 34, further comprising a plurality of further diffusion regions of the second conductivity type in the further charge barrier well adjacent to the charge sink and forming a plurality of transistors, wherein the plurality of transistors ~~include~~ includes a reset transistor and an emitter follower amplifier, both coupled to the charge sink.